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AUTOMATED ARRAY ASSEMBLY, PHASE II

R. V. D'Aiello
RCA Laboratories
Princeton, New Jersey 08540

QUARTERLY REPORT NO. 6

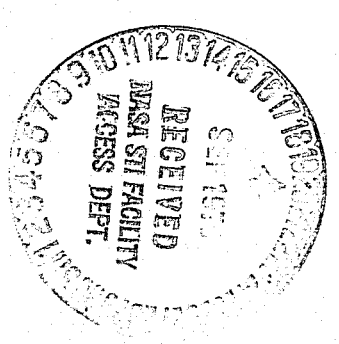
JUNE 1979

This work was performed for the Jet Propulsion Laboratory, California Institute of Technology, under NASA Contract NAS7-100 for the Department of Energy.

The JPL Low-Cost Silicon Solar Array Project is funded by DOE and forms part of the DOE Photovoltaic Conversion Program to initiate a major effort toward the development of low-cost solar arrays.

Prepared Under Contract No. 954868 For

JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE OF TECHNOLOGY
Pasadena, California 91103



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PREFACE

This Quarterly Report, prepared by RCA Laboratories, Princeton, NJ 08540, describes the results of work performed from April 1, 1979 to June 30, 1979 in the Energy Systems Research Laboratory, B. F. Williams, Director; Materials and Process Laboratory, Solid State Division, Somerville, NJ, R. Denning, Manager; and at the Advanced Technology Laboratory, Government and Commerical Systems, Camden, NJ, F. E. Shashoua, Director. The Project Scientist is R. V. D'Aiello and the Project Supervisor is A. H. Firester, Head, Process and Applications. Others who participated in the research and writing of this report are:

E. C. Douglas	-	Ion implantation
J. Murr	-	Screen printing
W. Kern	-	Spray-on AR coating
J. Toner	-	Cost analysis
R. Scott P. Coyle	-	Interconnect and panel assembly
L. Guarino	-	Processing
G. Nostrand	-	Cell testing and test system design

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SECTION I

SUMMARY

This is the sixth quarterly report under contract 954868, which is being performed for JPL-LSA, Task IV project to analyze and evolve cost-effective manufacturing processes for the large-scale production of silicon solar-cell array panels. The results reported here were obtained during the second quarter of a phase of activity directed toward a cost and performance evaluation of three manufacturing sequences designed to convert silicon sheet and wafers into solar panels.

Work during the second quarter centered around production studies of ion-implanted and furnace-annealed solar cells made using "solar-grade" n- and p-type wafers. The performance of production-size lots was examined with regard to the relationship between the ion-implant and furnace-anneal parameters and the ability to form consistently good thick-film screen-printed contacts. Initial results indicate that the implant dose must be increased to about twice our design value so that the resultant sheet resistance of the junction layer is less than 50 Ω/□. Reasonably good contacts with screen-printed metallization could only be obtained for such junction layers.

Evaluations of the spray-on AR coating process using a production model 9000 Zicon* autocoater have continued. Several lots of cells were coated, and performance before and after coating was measured. In addition, analytical studies were performed to determine and compare the structure and refractive index of the RCA I (TiO_2) coating with commercial solutions. Sensitivity of coated, screen-printed cells to the post-heat treatment required to cure the films was also assessed.

The double-glass lamination technique has continued, and two 4x4-ft panels were successfully fabricated during this quarter. These panels along with several smaller ones have been framed and are now ready for testing.

The automatic electrical test system which was designed and assembled during the first quarter was tested for the absolute measurement of cell parameters by making comparative measurements on previously calibrated standard cells. We have also added a subroutine to make temperature corrections to the measured cell parameters.

*Zicon Corp., Mt. Vernon, NY.

SECTION II

INTRODUCTION

In our previous work, we have identified cost-effective processes for large-scale silicon solar-panel production, brought those processes needing development to a state of technological readiness, and verified each process by experimental production of solar cells and panels. A selling price of less than $500/kW requires that these processes be assembled to form a manufacturing sequence with internal compatibility and the capability of operating at the estimated high throughput and yield.

In this present program, three such manufacturing sequences shown in Figs. 1 and 2 were selected and will be evaluated and compared on the basis of their cost/performance effectiveness. This evaluation will be performed by studying the production flow for each sequence involving the processing of 2420 solar cells, which will be used in the fabrication of 20 solar panels. The present production plan includes the fabrication of 1040 cells of the 2420 cells from EFG ribbon and web silicon* with the remainder made in "solar-grade"** so that we can evaluate and gain experience in the handling of sheet silicon and test the sensitivity of these sequences to the starting silicon characteristics.

*EFG ribbon to be purchased from Mobil-Tyco Solar Energy Corp., Waltham, MA. Web silicon to be purchased from Westinghouse Research and Development Center, Pittsburgh, PA. The quantity of cells and production scheduling depend on the delivery schedule from these vendors.

**"Solar-grade" silicon is a product of the Monsanto Corp., St. Louis, MO. These are 3-in.-diameter n- or p-type, 1/2 to 2 Ω-cm, round silicon wafers, received in a "saw-cut" form.

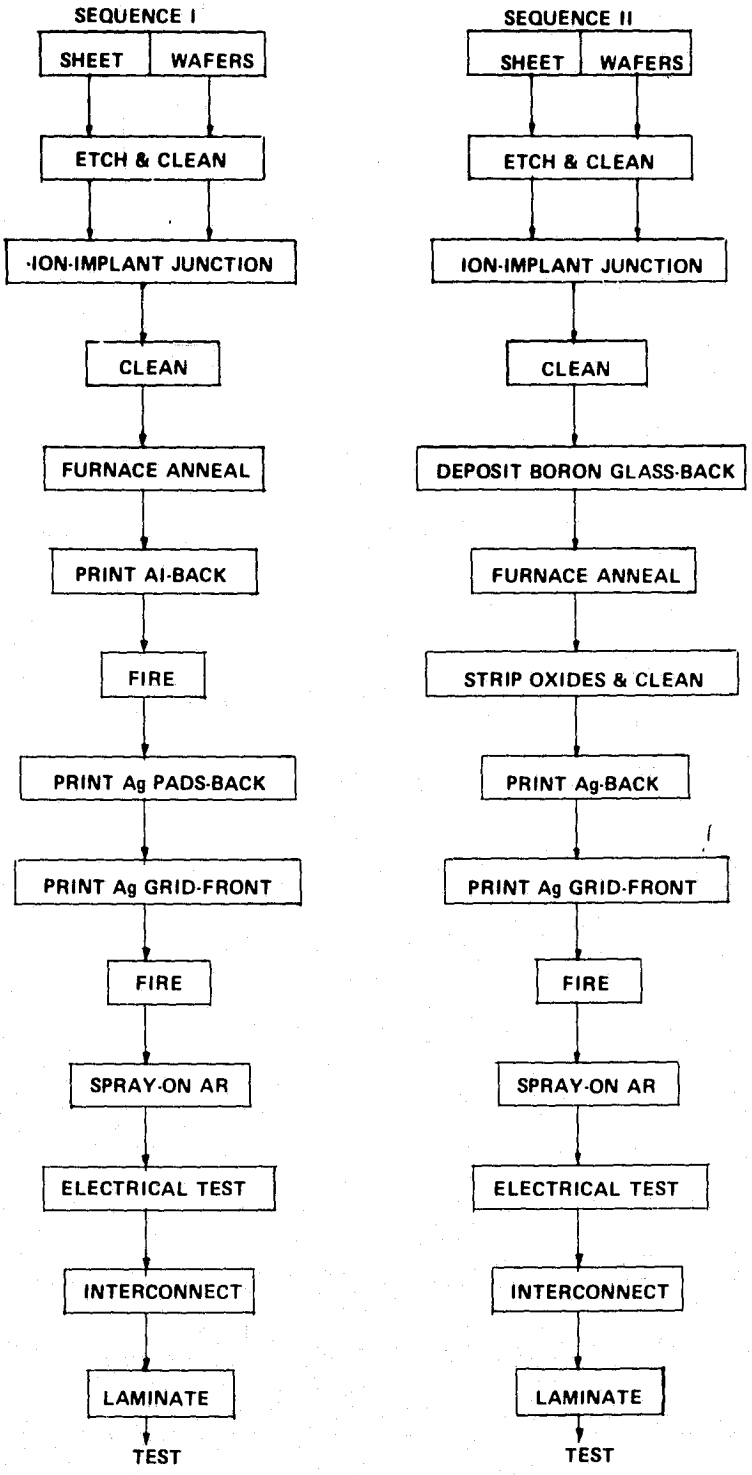

Figure 1. Manufacturing sequences I and II.

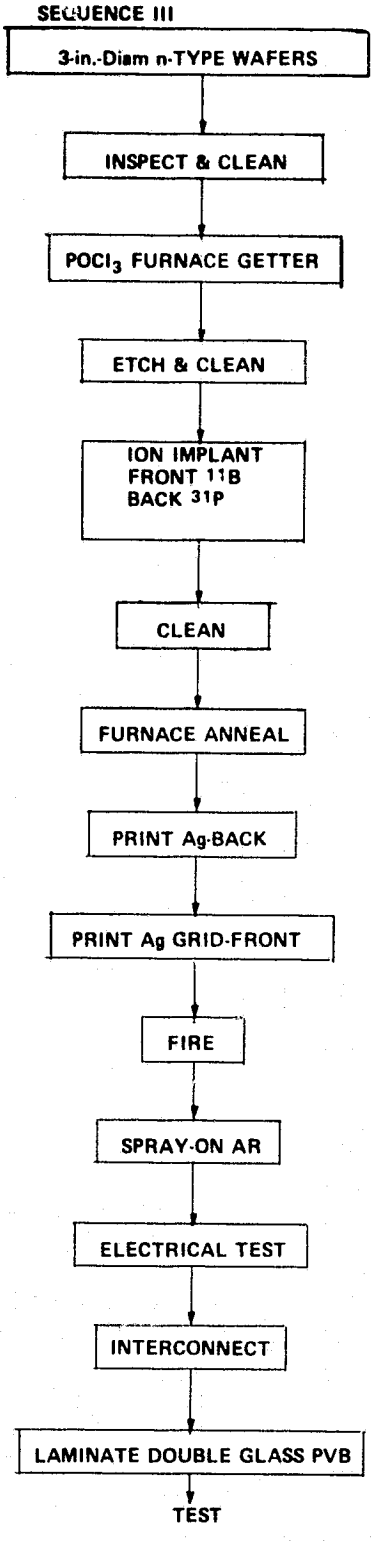

Figure 2. Manufacturing sequence III.

SECTION III

PROGRESS

A. SOLAR-CELL PROCESSING

The following sections deal with tests conducted to assure the proper operation of equipment, some results which relate to the production of ion-implanted solar cells, and a description of the performance of such cells made in accordance with the manufacturing sequences described in Section II.

1. Equipment and Process Qualification

Preliminary to running ion-implanted solar cells of sequences I, II, and III through production-model screen printing and spray-on AR coating, these processes were tested on 3-in.-diameter solar-cell wafers containing a junction formed by $POCl_3$ diffusion. This was done because the performance level of such cells had previously been established on laboratory versions of this equipment.

These tests were performed on a group of 37, 3-in.-diameter solar-cell wafers split into two lots containing 12 and 25 cells. In the first lot of 12 wafers, six were screen printed on the sun-side with a previously used grid pattern having 14% shadowing and six with our new grid design [1] (9% shadowing). In the second lot, all wafers were printed with the new mask. In all cases, TFS* 3347 silver ink was used on the junction side and RCA p-type [2] on the back (84% coverage on the back). Examination of the new grid pattern after printing revealed good line definition; the minimum designed line width (0.005 in.) printed with an average width of 5-1/2 mil. After firing at 675°C for 2 min between dual infrared lamps, these lines slumped at the edges, yielding a line of ∿0.006-in. width.

After firing, the AM-1 illuminated cell parameters were measured, and the statistical results comparing grid patterns are summarized in Table 1. The cell characteristics for both patterns are very good; for the new grid, no significant reduction in fill factor was experienced, and a 6% increase in short-circuit

1. R. V. D'Aiello, Automated Array Assembly, Phase II, Quarterly Report No. 5, prepared under Contract No. 954868 for Jet Propulsion Laboratory, DOE/JPL-954868-79/2, March 1979.
2. R. V. D'Aiello, Automated Array Assembly, Phase II, Quarterly Report No. 4, prepared under Contract No. 954868 for Jet Propulsion Laboratory, DOE/JPL-954868-78/4, October 1978.

*Thick Film Systems, Inc., Santa Barbara, CA.

TABLE 1. AVERAGE AND STANDARD DEVIATION FOR ALL PARAMETERS OF SCREEN-PRINTED CELLS

Grid Pattern	$\overline{J_{sc}}$ (mA/cm^2)	σ_j (mA/cm^2)	$\overline{V_{oc}}$ (mV)	σ_v (mV)	$\overline{FF}$ -	σ_F -	$\bar{\eta}$ —	σ_n —	$J_{sc\ max}$ (mA/cm^2)	$V_{oc\ max}$ (mV)	FF_{max} -	η_{max} (%)
OLD (No AR)	19.9	0.57	588	4.5	0.763	0.008	8.89	0.30	20.9	592	0.769	9.33
NEW (No AR)	21.1	0.65	593	3.1	0.754	0.017	9.37	0.22	21.6	599	0.771	9.56

*Cell area = 41 cm^2

current was obtained, as expected. Similarly good results were obtained on the 25-wafer lot as illustrated in the following data:

$\overline{J_{sc}}^{*}$	σ_j	$\overline{V_{oc}}$	σ_v	$\overline{FF}$	σ_F	$\bar{\eta}$	σ_n	$J_{sc\ max}$	$V_{oc\ max}$	FF_{max}	η_{max}
(mA/cm^2)	(mA/cm^2)	(mV)	(mV)	-	-	(%)	(%)	(mA/cm^2)	(mV)	-	(%)
20.7	0.35	579	2.1	0.761	0.007	9.23	0.15	21.5	586	0.772	9.66

*Cell area = 42 cm^2, no AR coating.

These cells were spray AR coated with the RCA I TiO_2 solution using the Zicon Model 9000 autocoater as previously described [1]. Typical results before and after coating are shown in Table 2. The coated-cell parameters are reasonably good; however, the uniformity and film quality were found to be sensitive to the ambient relative humidity (RH) for values of RH greater than ~45%.

TABLE 2. COMPARISON OF AVERAGE AM-1 PARAMETERS BEFORE AND AFTER SPRAY AR COATING

	$\overline{J_{sc}}$	$\overline{V_{oc}}$	$\overline{FF}$	$\bar{\eta}$	$J_{sc\ max}$	$V_{oc\ max}$	FF_{max}	η_{max}
	(mA/cm^2)	(mV)	-	(%)	(mA/cm^2)	(mV)	-	(%)
Before	21.1	593	0.754	9.37	21.6	599	0.771	9.56
After	28.7	601	0.752	12.65	29.3	610	0.761	13.2

These tests have established the material requirements and operating conditions for the screen-printing and spray-on AR coating processes.

2. Ion Implantation and Furnace Annealing

The manufacturing sequences described in Section II require the formation of a junction by ion implantation and furnace annealing. A lot of 100 "solar-grade" wafers was processed through ion implantation and furnace annealing, and the distribution of junction-layer sheet resistances was measured prior to screen printing the contacts. These wafers were implanted with 2 x 10^{15} A/cm^2, ^{31}P followed by a three-step (500°C, 2 h; 850°C, 30 min; 500°C, 2 h) furnace anneal. The distribution of measured sheet resistances is shown in Fig. 3. Both the average value (95 Ω/□) and the spread are higher than previously experienced under similar dose and furnace conditions. However, ion-implanted layers are normally capped with an SiO_2 film to prevent impurity contamination

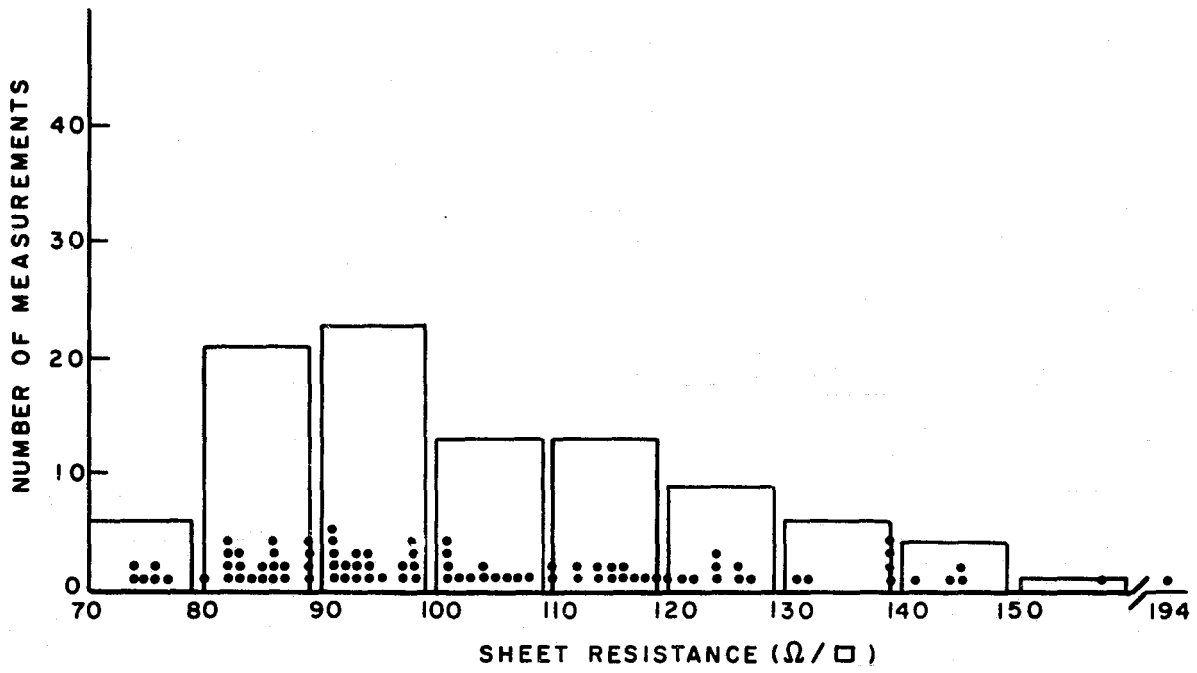

Figure 3. Distribution of sheet resistance for lots 950, 951, and 952.

and/or out-diffusion of the phosphorus during the high-temperature anneal, and these wafers were not capped because the capping step was not considered to be cost-effective.

The wide range (75 to 194 Ω/□) of sheet resistance values made this lot suitable for testing the sensitivity of the screen-printing and firing process to the absolute value of sheet resistance. Twenty-five wafers were selected from the lot and were screen-printed and fired as described in subsection III.A.1 above. The cell characteristics were measured and are listed in Table 3 along with the sheet-resistance values for each cell. It is seen from these data that the fill factors are low and decrease almost monotonically with increasing sheet resistance as shown in Fig. 4. The grid metallization pattern is designed for sheet resistivities slightly greater than 100 Ω/□. Thus, the effect shown in Fig. 4 is not due simply to the increased sheet resistivity, but rather results from the interaction of the present screen-printed metallization process and the silicon surface resistivity.

It can be concluded from these data that junction layers formed in solar-grade wafers with a phosphorus dose of 2×10^{15} A cm^{-2} and annealed in the manner described are not compatible with the present thick-film screen-printing process.

TABLE 3. AM-1 PARAMETERS FOR LOTS 950, 951, and 952

CELL NUM	OPEN CIR VOLT	CELL CURRENT	MAX POWER	FILL FACT	SER RESIS	SHUNT RESIS	PMAX CURRENT	PMAX VOLT	EFF	BASE TEMP
D1NS950001	.531	826.	6.47	.620	.107	11.40	707.	.384	.066	27.3
D1NS950003	.518	810.	6.05	.606	.114	19.80	680.	.373	.061	27.3
D1NS950004	.514	790.	5.52	.571	.137	399.00	650.	.357	.056	27.8
D1NS950005	.527	780.	5.94	.607	.121	22.60	639.	.390	.060	27.9
D1NS950006	.533	785.	6.00	.603	.127	7.21	645.	.391	.061	28.2
D1NS950007	.527	821.	5.88	.572	.128	99.00	651.	.380	.060	28.2
D1NS950008	.525	782.	5.31	.595	.126	11.20	636.	.384	.059	28.3
D1NS950009	.531	803.	5.85	.576	.140	6.37	648.	.379	.060	28.3
D1NS950010	.512	808.	5.58	.567	.131	32.30	637.	.368	.057	28.3
D1NS951001	.528	796.	5.67	.568	.139	8.74	619.	.385	.058	27.8
D1NS951002	.426	859.	4.25	.488	.174	4.07	652.	.274	.044	28.0
D1NS951003	.324	742.	1.92	.336	.298	.76	449.	.179	.020	28.1
D1NS951004	.518	855.	5.26	.499	.164	12.90	617.	.358	.054	28.2
D1NS951005	.506	820.	5.20	.527	.146	8.70	609.	.359	.053	28.3
D1NS952001	.521	832.	4.78	.464	.223	3.35	600.	.335	.049	27.9
D1NS952002	.512	839.	5.03	.492	.162	7.56	631.	.335	.052	28.3
D1NS952003	.405	870.	4.09	.467	.162	3.34	654.	.263	.042	28.3
D1NS952004	.426	873.	4.09	.464	.191	4.48	654.	.263	.042	28.4
D1NS952005	.495	836.	4.60	.467	.191	4.53	597.	.324	.047	28.5
D1NS952006	.497	804.	4.49	.472	.206	3.80	532.	.324	.046	28.4
D1NS952007	.510	799.	4.75	.490	.195	6.36	595.	.335	.049	28.5
D1NS952008	.463	866.	4.66	.490	.171	3.16	637.	.307	.048	28.5
D1NS952009	.275	848.	2.31	.417	.162	2.62	574.	.169	.025	28.7

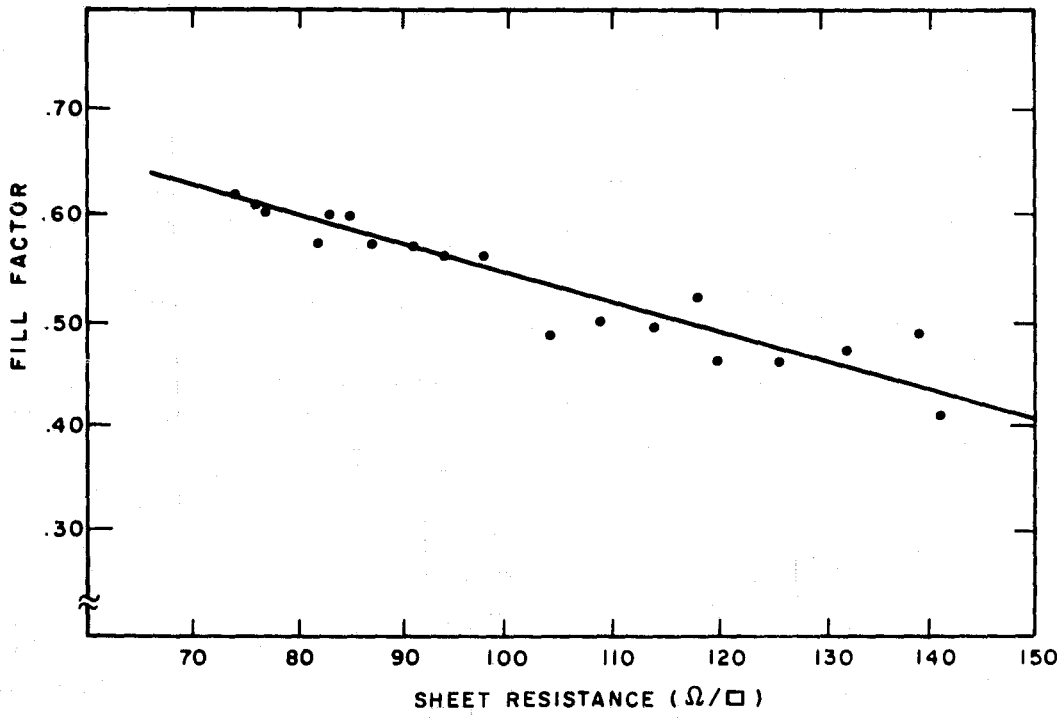

Figure 4. Measured fill factor as a function of sheet resistance for lots 950, 951, and 952.

The results of increasing the phosphorus dose level and adjustments in the annealing temperature are described below.

3. Manufacturing Sequences

Based on the results described above, adjustments were made in the phosphorus dose and/or anneal schedule in order to reduce the resultant sheet resistance of the junction layer. Three lots of 25 wafers each were formed; Table 4 shows the conditions for furnace annealing and ^{31}P dose along with the average sheet resistance obtained after annealing. Figures 5, 6, and 7 show that the spread in the distribution of measured sheet resistance is very much less than that obtained with both a lower ^{31}P dose and anneal temperature as described in subsection III.A.2 above (see Fig. 3).

TABLE 4. ^{31}P DOSE AND ANNEAL CONDITIONS FOR THREE LOTS OF SOLAR-CELL WAFERS

Lot No.	^{31}P Dose (A/cm^2)	Furnace Anneal	$\bar{R}_{\square}$ ($\Omega/\square$)
107P	$4x10^{15}$	L* 850°C L 30 min	58
106P	$4x10^{15}$	L 950°C L 30 min	34
910P	$2x10^{15}$	L 950°C L 30 min	52

*L = 500°C, 2 h

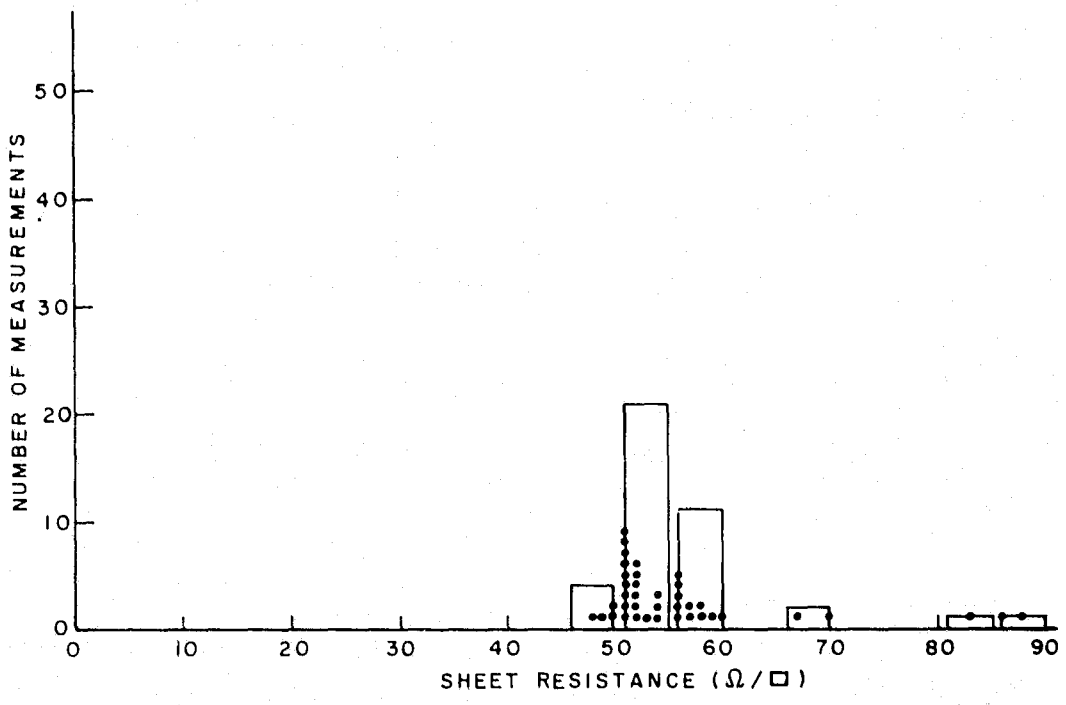

Figure 5. Distribution of sheet resistance for wafers of lot 907P.

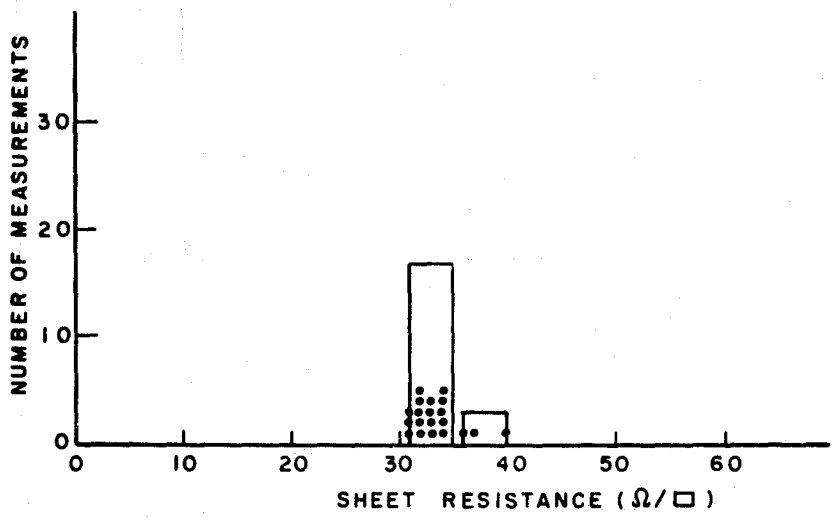

Figure 6. Distribution of sheet resistance for wafers of lot 106P.

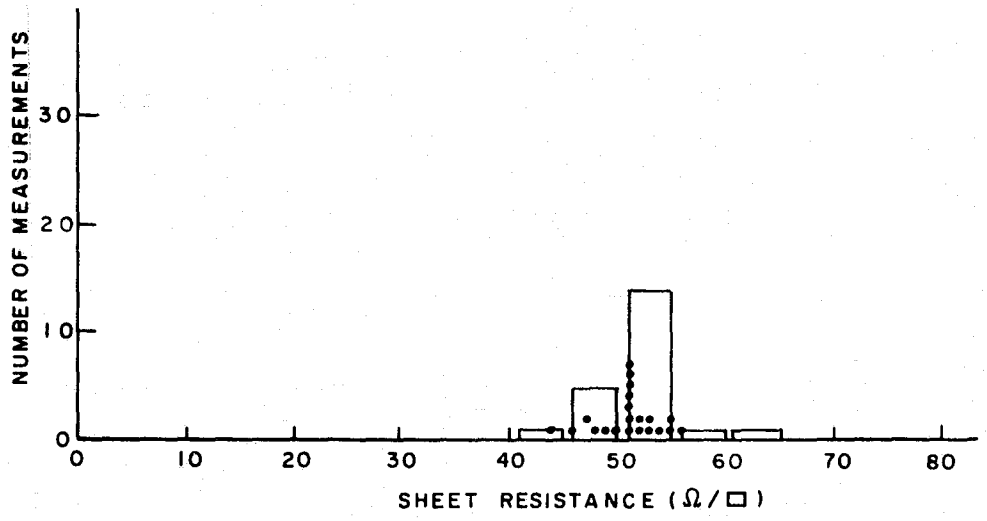

Figure 7. Distribution of sheet resistance for wafers of lot 910P.

After screen printing and firing, the cell characteristics for the three lots were measured. Table 5 lists the average values of the AM-1 illuminated cell parameters along with the average for lots 950, 951, and 952. Clearly, a significant improvement in cell characteristics, especially in the fill factor, is obtained when the surface layer sheet resistance is lowered. It is interesting to compare the fill factors obtained on all lots processed as an

extension to the data shown in Fig. 4. In Fig. 8, an extended linear fit to the data of Fig. 4 is shown and data points showing the average value of fill factor for all other lots are plotted.

TABLE 5. AVERAGE AM-1 ILLUMINATED CELL PARAMETERS FOR THE WAFER LOTS OF TABLE 4

Lot No.	$\overline{J_{sc}}$ (mA/cm^2)	$\overline{V_{oc}}$ (mV)	$\overline{FF}$ -	$\overline{\eta}$* (%)	$\overline{R_{\square}}$ (Ω/□)
107P	21.7	552	0.659	7.9	58
106P	20.7	557	0.710	8.2	34
910P	20.5	560	0.700	8.0	52
950 - 952	19.5	499	0.518	5.1	75-150

*No AR Coating

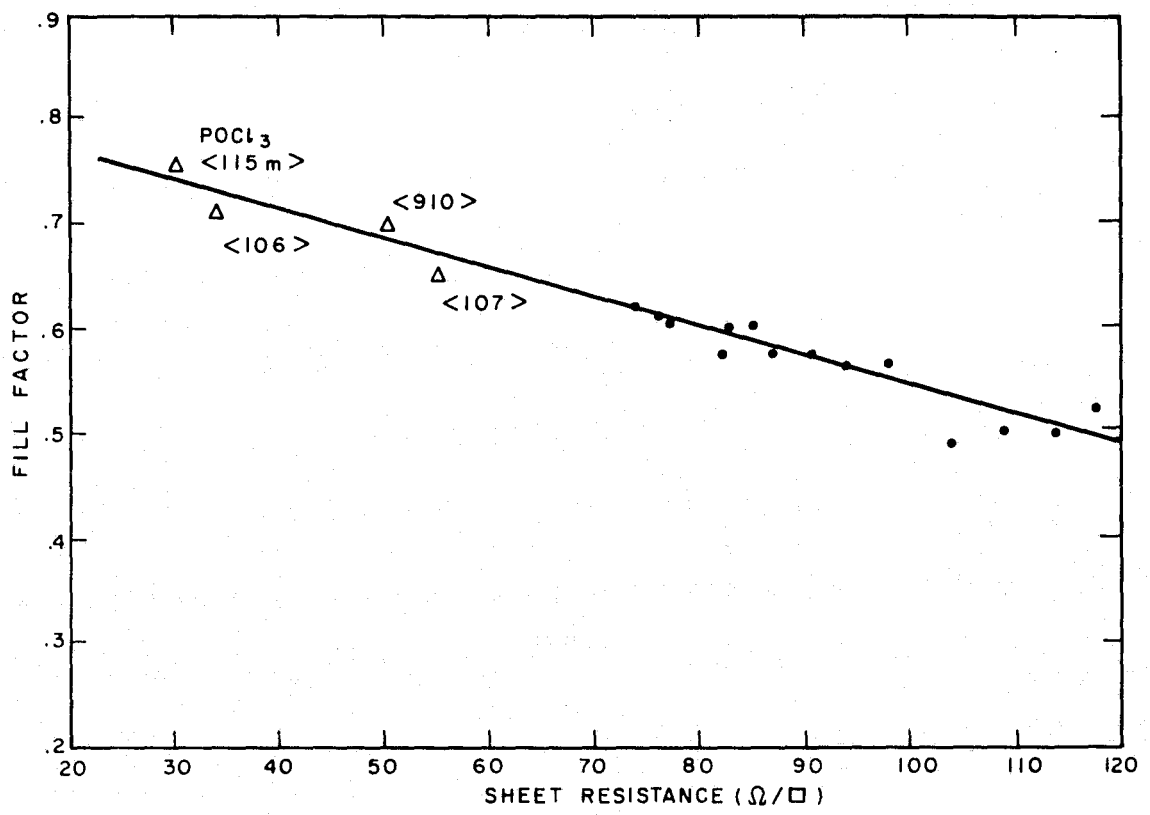

Figure 8. Fill factor as a function of sheet resistance including average values for lots 106, 107, 910, and 115m.

B. SPRAY-ON AR COATING PROCESS

1. Spray-on AR Process Applied to Solar Cells

The model 9000 Zicon autocoater was used to spray the RCA I AR coating solution on several lots of cells described in the previous section. Typical values of short-circuit current before and after the AR coating process are given in Table 6. The average increase in short-circuit current is +31% which is 4% lower than our previous experience [2]. Some nonuniformity in film thickness was noted, especially near the metal, causing individual values (samples 910-7 and 910-12) to be lower than expected.

2. Physical and Optical Properties of Spray-on AR Films

Additional analyses have been carried out to determine the structure and refractive index of the RCA I derived TiO_2 (more realistically TiO_x) coating and the Emulsitone* C TiO_2-SiO_2 coating as a function of heat-treatment time at 400°C. Electron diffraction indicated an amorphous structure of the TiO_2-SiO_2 coating and of the TiO_x coating heated for only 30 s which is our normal heat treatment. After the TiO_x film was heated for 5.5 and 55 min, a crystalline TiO_2 phase appeared which was identified as Anastase. The refractive index was measured by ellipsometry. These results are presented graphically in Fig. 9. The TiO_x film reaches a constant refractive index value of 2.22 after the 5.5- or 55-min heat treatment, indicating a stable film structure. The TiO_2-SiO_2 film, on the other hand, keeps increasing in refractive index with heating time.

Absolute reflection of the RCA I TiO_x coating on polished silicon slices as a function of wavelength for the 30-s heat-treatment period is shown in Fig. 10. A broad reflection minimum of 1.3% is reached at a wavelength of 6000 Å. A measurement of the transmittance of the coating on a quartz substrate gives a measure of the absorption. Such measurements for films heat-treated at 0.5, 5, and 50 min are shown in Fig. 11 where it can be seen that there is no significant absorption down to a wavelength of 0.37 μm.

*Emulsitone Company, Whippany, NJ.

TABLE 6. SHORT-CIRCUIT CURRENT BEFORE AND AFTER SPRAY AR PROCESS FOR LOT 910

Cell No.	$I_{sc\ No\ AR}$ (mA)	$I_{sc\ AR}$ (mA)	$\Gamma = \frac{I_{sc\ AR}}{I_{sc\ No\ AR}}$ -
910 - 1	875	1170	1.34
910 - 2	870	1150	1.32
910 - 3	890	1180	1.33
910 - 4	842	1090	1.29
910 - 5	848	1170	1.38
910 - 6	869	1150	1.32
910 - 7	906	1150	1.27
910 - 8	871	1140	1.31
910 - 9	849	1110	1.31
910 - 10	864	1200	1.39
910 - 11	870	1050	1.21
910 - 12	909	1150	1.27
910 - 13	875	1170	1.34
910 - 14	881	1130	1.29
			Ave. 1.31

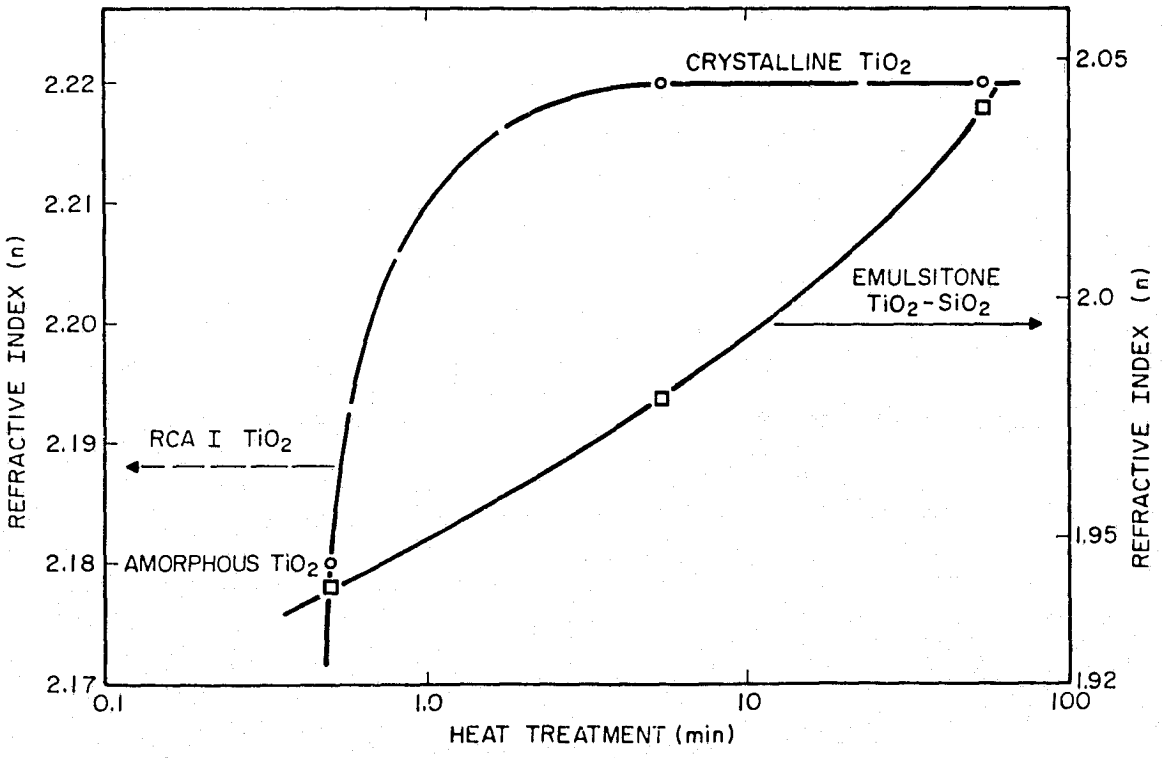

Figure 9. Refractive index vs heat treatment time at 400°C.

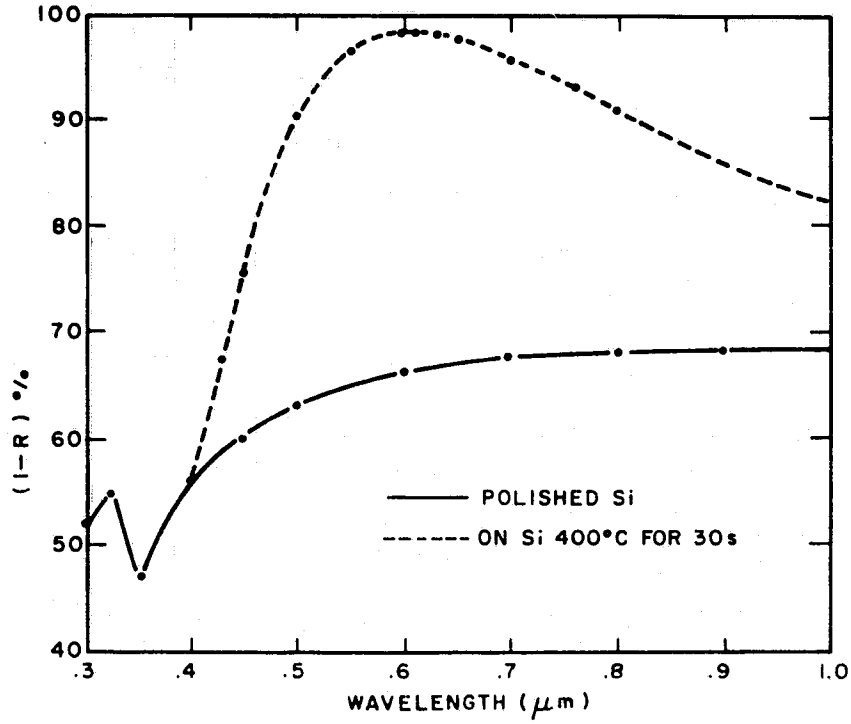

Figure 10. Reflection spectrum for spray-on AR film on silicon.

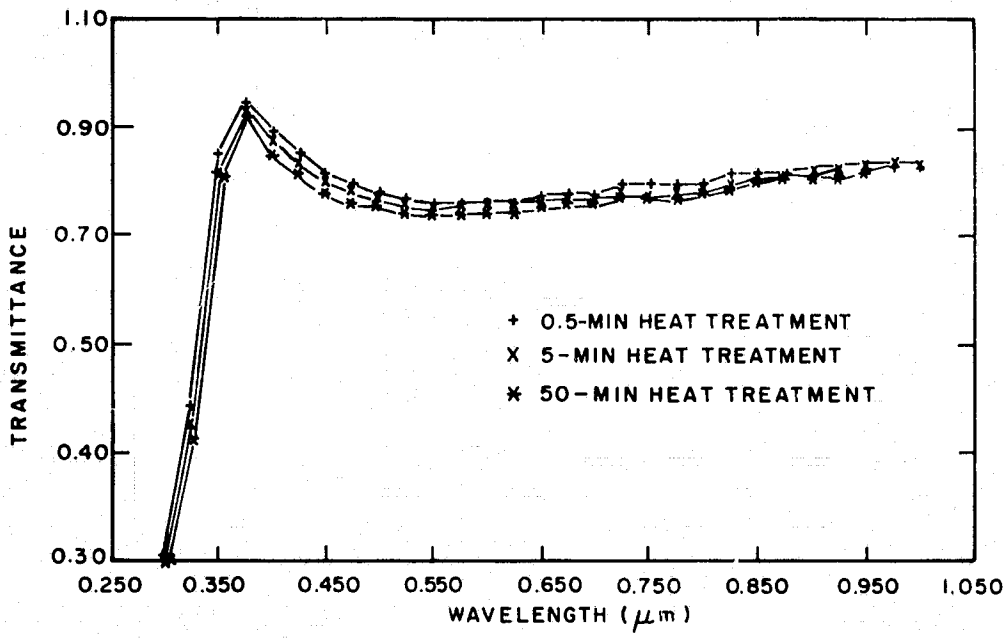

Figure 11. Transmittance data.

3. Effect of Curing Cycles on Cell Properties

To cure the spray-on AR films, our normal heat-treatment cycle is 30 s each at 70, 200, and 400°C in air. To assess the sensitivity of cell properties to heat treatment, five screen-printed and AR-coated cells and three uncoated cells were heated at 400°C for times ranging from 0.5 to 15 min. The results of this test are given in Table 7. These results show:

- The AR film is unaffected by extended heat treatment.
- Degradation in cell properties is not related to the AR film and is confined to reduction of the fill factor and does not begin until after 3 min of heat treatment at 400°C.
- Spray-coated cells show less degradation than uncoated cells.

TABLE 7. EFFECT OF HEAT TREATMENT ON SPRAY AR COATED AND UNCOATED CELLS

Cell No.	Spray AR	Time at 400°C (min)	I_{SO} (mA)	I_{ST} (mA)	Comments
115m - 1	Yes	1.0	1100	1091	No significant change
115m - 2	Yes	2.0	1110	1093	No significant change
115m - 3	Yes	3.0	1100	1095	No significant change
115m - 4	Yes	5.0	1090	1086	Small reduction in FF 0.760 → 0.737
115m - 5	Yes	15.0	1130	1123	Seriously degraded 0.761 → 0.600
115m - 6	No	2.0	900	900	No change
115m - 7	No	5.0	895	890	Fill factor severely degraded 0.755 → 0.591
115m - 8	No	15.0	895	895	Fill factor severely degraded 0.751 → 0.570

C. PANEL ASSEMBLY

1. Panel Lamination and Framing

Successful double-glass laminations have been achieved for two 4x4-ft panels and four 1x4-ft panels containing live arrays of interconnected cells.

A description of these panels and the procedures used in the lamination were given in Quarterly Report No. 5 [1]. During this quarter, the framing technique also described in that report was applied to these panels.

Framing for both large and small panels has been accomplished. The concept calls for eventually using an extruded section that will be flash-welded at the corners of the frame. After a glass panel has been placed in the frame, the edges will be rolled over (Fig. 12).

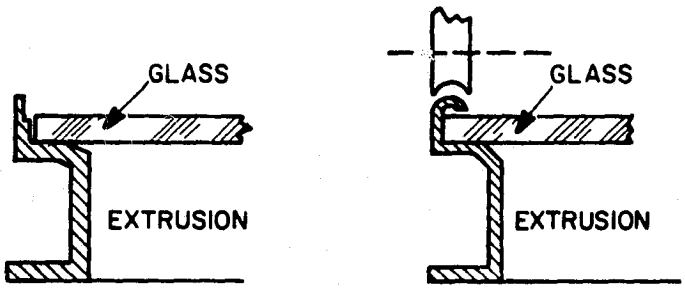

Figure 12. Framing concept showing roll-over extrusion.

The rolling process will have to be tailored to avoid breakage of the glass; however, the edge to be rolled can be relatively thin and yet provide sufficient retaining force.

Frame samples are shown in Figs. 13, 14, and 15. These frames simulate the rolled edges by use of a thin-walled C-section (Fig. 16).

The frame in Fig. 15 was arc-welded at the corners, while that in Fig. 14 was bolted. Either design is feasible as a final product; however, both would cost significantly more than the structure as conceived in Fig. 12.

A method of external interconnection was implemented for evaluation. The scheme consists of providing an insulated standoff at opposite corners (Fig. 17) rather than a pigtail lead. With this system, cables can be provided to whatever length desired, as a separate item.

The standoffs can be supplied as either male or female fittings (male type shown here), and the mating cables are assumed to have rubber caps as integral fittings. Obviously, the accumulated years of experience of the automotive industry with ignition systems would suggest that this is a viable system.

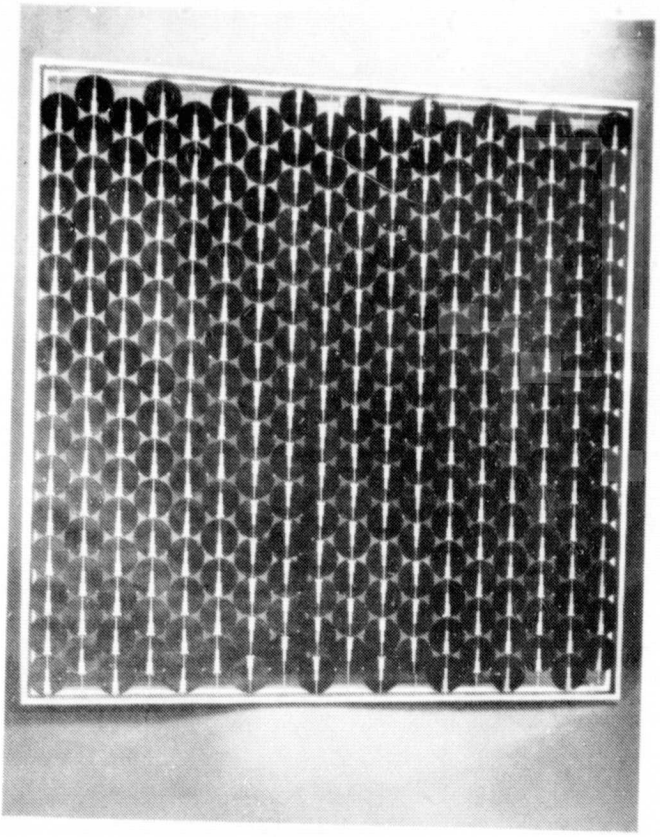

Figure 13. Frame sample.

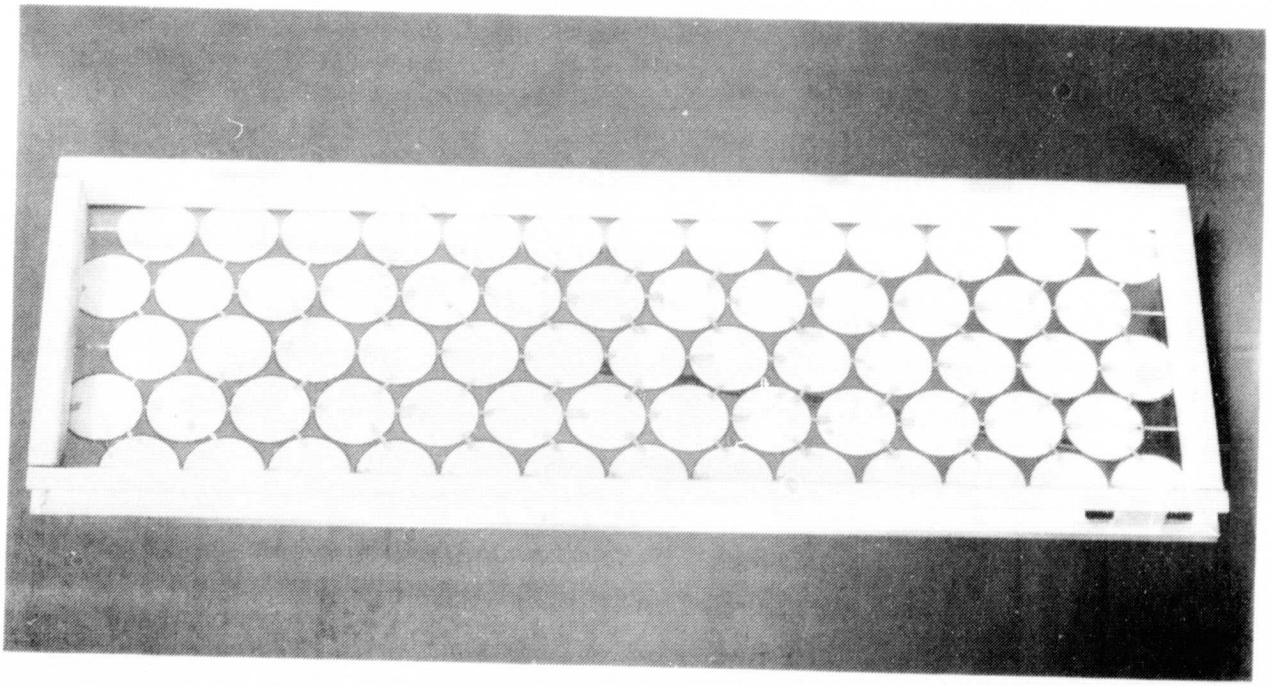

Figure 14. Frame bolted at the corners.

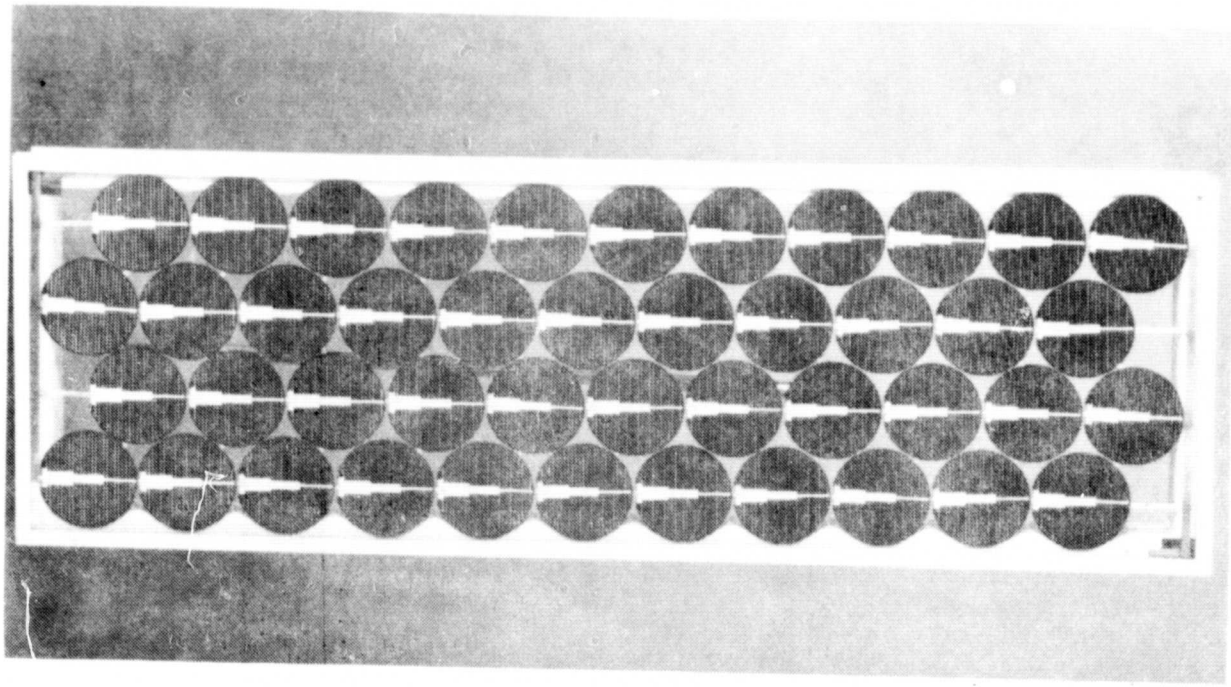

Figure 15. Frame arc-welded at the corners.

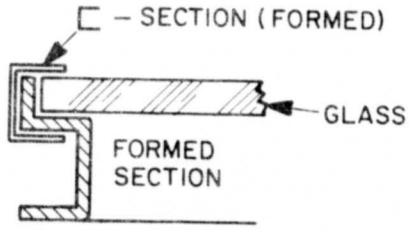

Figure 16. Framing concept showing C-section.

2. Radiant-Heat Mass Reflow Soldering Assembly

An experimental radiant soldering assembly was designed and constructed. The purpose is to demonstrate the simultaneous reflow soldering of the cell interconnects of a 15x6 cell array. Figures 18 and 19 show the completed assembly; Fig. 20 shows the vacuum platen for handling the loose array as it is built up.

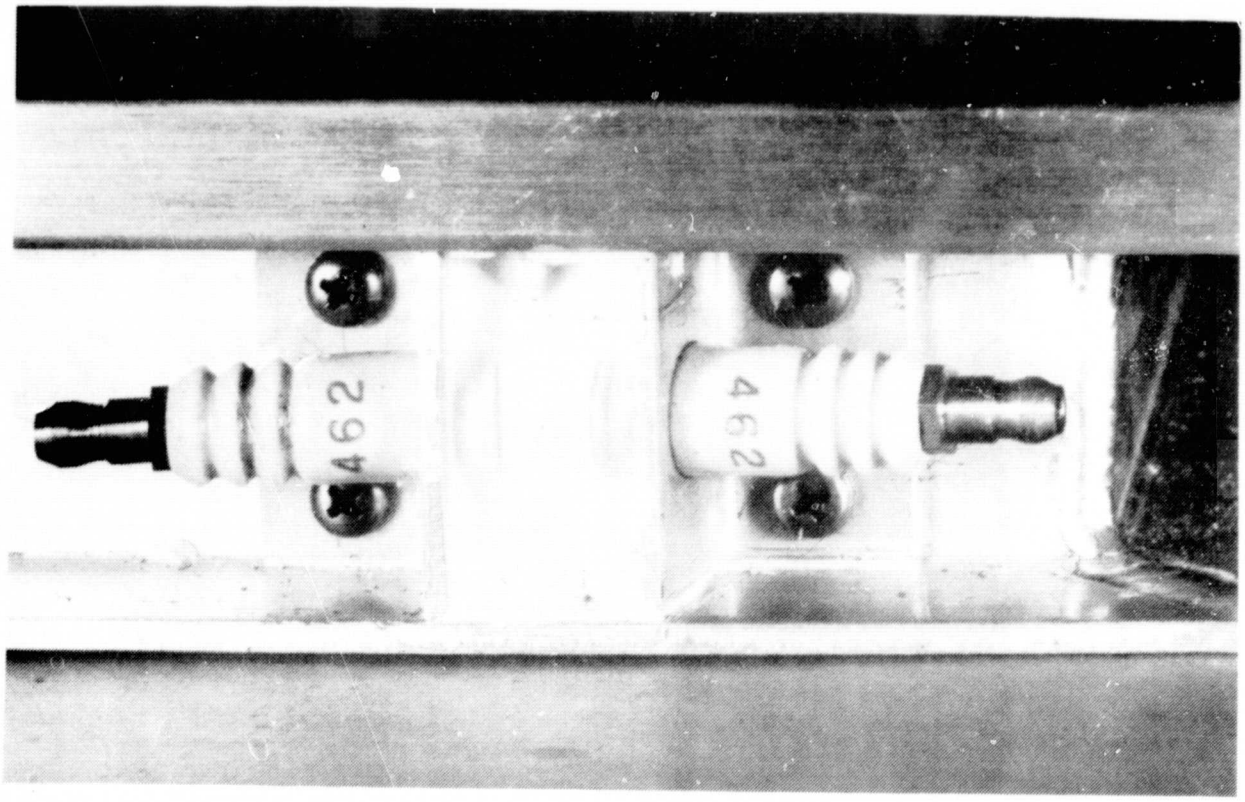

Figure 17. Insulated standoff at corners of frame.

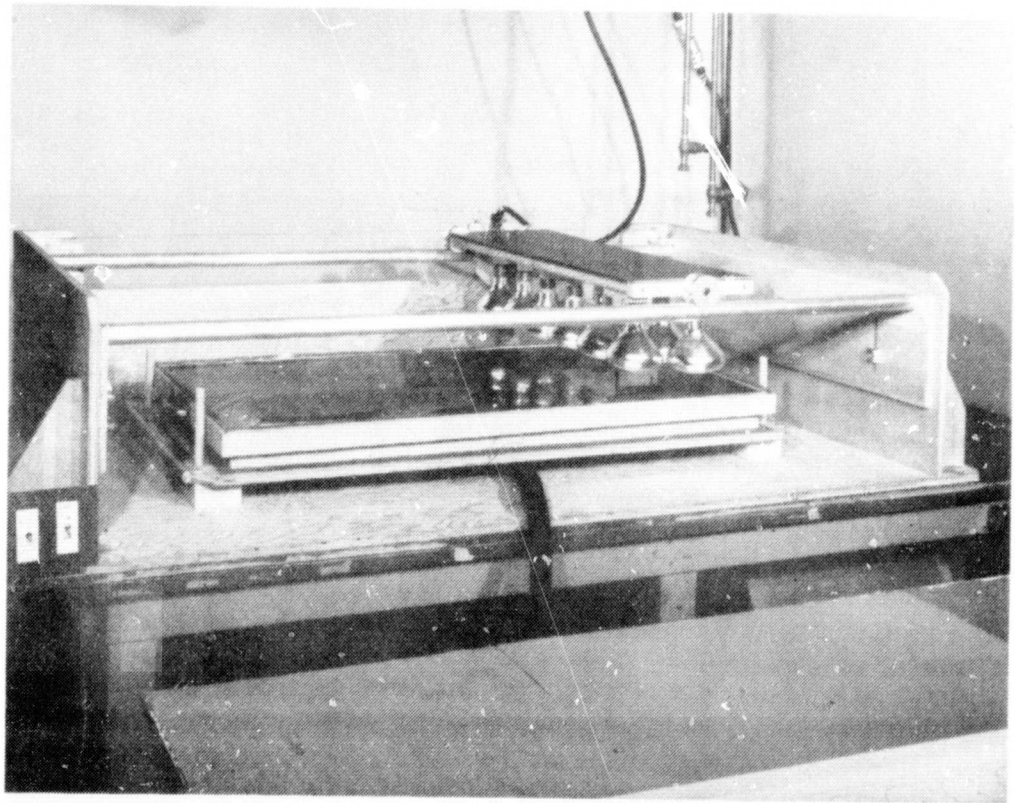

Figure 18. Radiant-heat mass reflow soldering assembly.

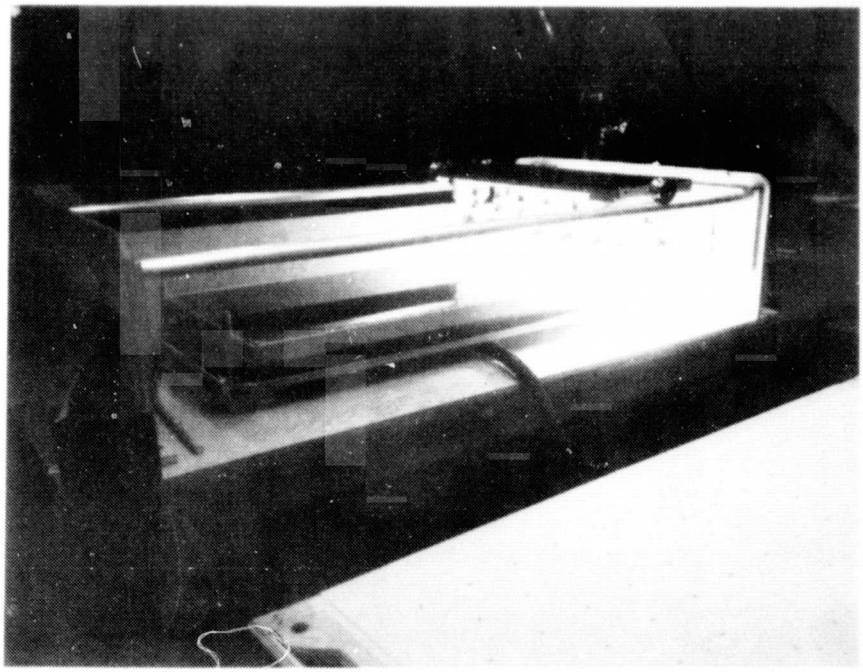

Figure 19. Radiant-heat mass reflow soldering assembly during processing.

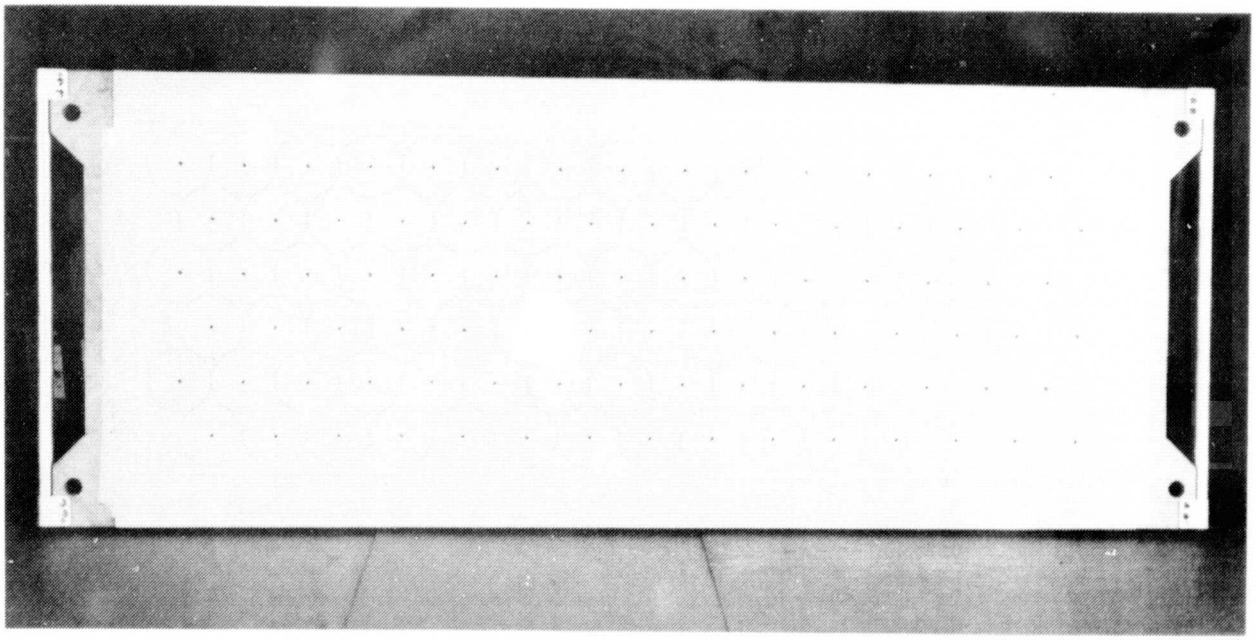

Figure 20. Vacuum platen for radiant soldering.

Soldering experiments will proceed as follows: each cell is first pre-tabbed (in production this would be done by machine) and laid down on the vacuum platen. The array is aligned by hand; the vacuum turned on; and the array transferred to the soldering fixture. The fixture has a second vacuum hold down with a silicone rubber liner. By placing the first platen over the second, with proper vacuum control, the cells are transferred to the rubber platen while maintaining alignment. They are then covered with a transparent kapton sheet which is held in position by the same vacuum system. At this point, each interconnect strap is securely held, mechanically, by being clamped between the rubber surface and cell, or by the kapton sheet and cell.

The bank of 18 heat lamps is then moved across the array at a rate such that heating of the cells causes the solder to melt for approximately 4 to 6 s.

This process yields uniform joints, with controlled film thickness (due to uniform pressure) and no solder bumps or spikes.

This assembly will be operationally tested during the first part of next quarter.

D. AUTOMATIC ELECTRICAL TEST SYSTEM

1. Qualification Test

The design and construction of a calculator-based automatic electrical test system for high-speed testing of solar cells was described last quarter [1]. In order to obtain accurate and reproducible values of cell parameters, the output illumination level from the Oriel* filtered xenon light source must be adjusted to the AM-1 level for each measurement. A better approach for high-speed measurements is to set the output level to AM-1, monitor it with a small standard cell, and correct the data for any change in light level. This latter approach was taken by placing a small (1.3 cm^2) silicon cell adjacent to the cell under test as shown in Fig. 21.

The initial level is set by using a calibrated silicon cell** and a set of measurements was made and compared to those obtained on a previously calibrated ELH lamp simulator. The results of such a comparison are shown in Table 8, where

*Oriel Corporation, Stanford, CT.
**Reference standard cell No. 49, provided by NASA Lewis Research Center, Cleveland, OH.

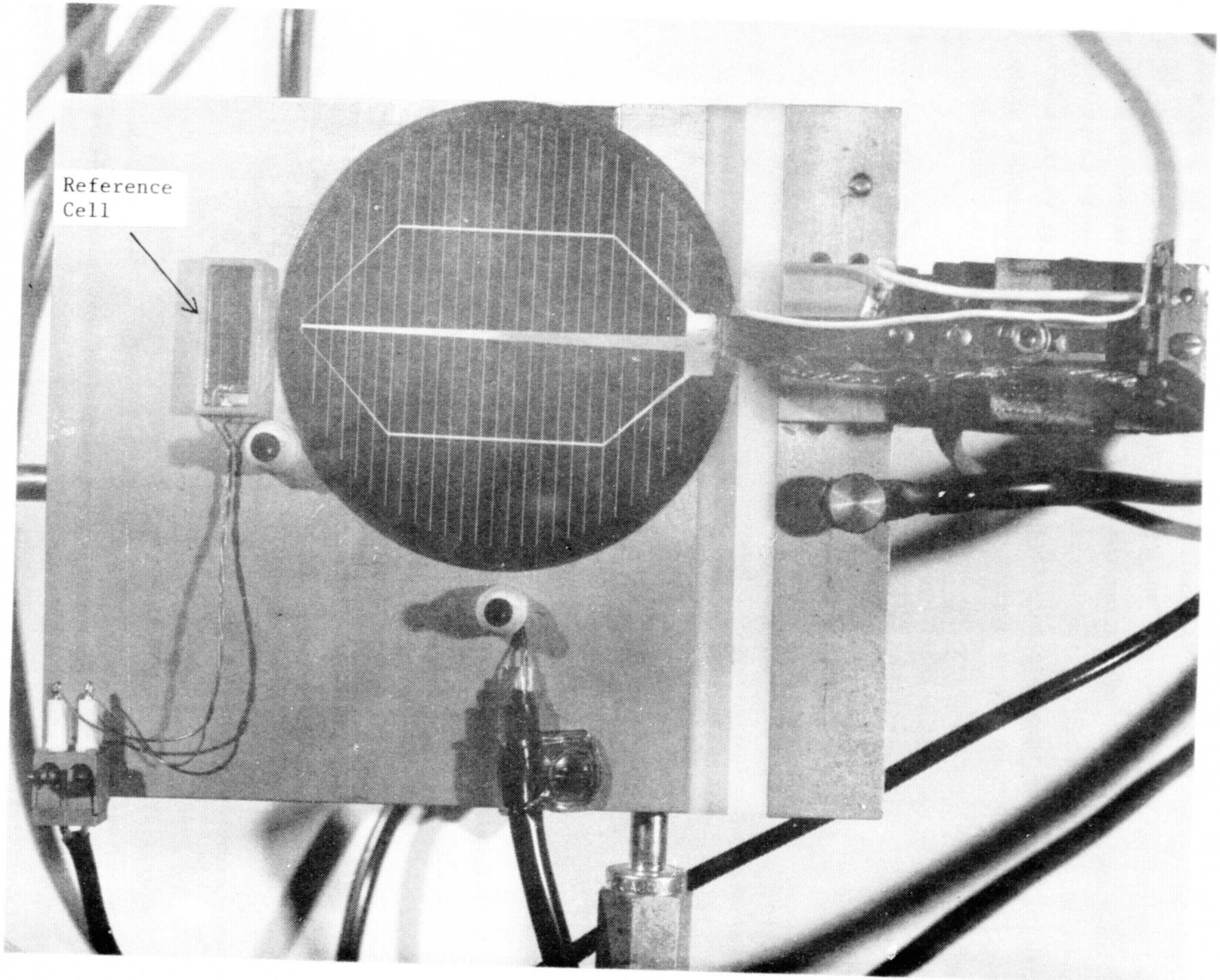

Figure 21. Photograph of cell-testing stage showing reference cell mounted adjacent to the cell under test.

it is seen that good agreement between the two sets of values was obtained. The difference in short-circuit current in all cases is less than 3.8%.

2. Temperature Corrections

The temperature beneath the cell under test is measured by means of a thermocouple permanently mounted in the stage. This value is recorded for each measurement and the cell parameters V_{oc}, FF and η are corrected back to 25°C using the following equations:

$$V_{ocT} = V_{oc} + S\ (T-25) \tag{1}$$

where $S = 0.002$ V/°C

$$EFF_T = \eta_T = \eta + \varepsilon\ (T-25) \tag{2}$$

where $\varepsilon = 0.04$ %/°C

and

$$FF = \frac{FF\ [1 + \varepsilon/\eta\ (T-25)]}{[1 + S/V_{oc}\ (T-25)]} \tag{3}$$

A typical set of measured and corrected parameters is illustrated in Table 9.

TABLE 8. COMPARISON OF CELL PARAMETERS ELH VS ORIEL AM-1 SIMULATION SYSTEM

Sample	V_{oc} (mV)	I_{sc} (mA)	V_m (mV)	I_m (mA)	FF -	η (%)
1 ELH	599	865	490	800	0.760	9.58
1 ORIEL	585	871	481	804	0.758	9.43
2 ELH	591	885	470	810	0.728	9.26
2 ORIEL	583	888	457	800	0.707	8.93
3 ELH	592	880	475	810	0.739	9.36
3 ORIEL	583	886	456	824	0.727	9.17
4 ELH	591	865	485	820	0.768	9.56
4 ORIEL	582	870	471	811	0.753	9.31
5 ELH	592	870	485	801	0.754	9.45
5 ORIEL	581	869	462	814	0.745	9.17
6 ELH	591	811	485	762	0.771	9.0
6 ORIEL	579	842	466	790	0.754	9.0
7 ELH	590	802	480	750	0.762	8.76
7 ORIEL	580	822	476	770	0.769	8.9
8 ELH	581	810	475	752	0.759	8.69
8 ORIEL	574	818	475	760	0.769	8.8
9 ELH	592	820	490	759	0.767	9.05
9 ORIEL	581	820	479	765	0.769	8.93
10 ELH	586	795	485	730	0.760	8.61
10 ORIEL	574	810	471	748	0.758	9.59
11 ELH	591	855	485	791	0.759	9.33
11 ORIEL	581	847	466	792	0.750	9.00

TABLE 9. TEMPERATURE CORRECTIONS OF CELL PARAMETERS

CELL NUMBER	VOC	VOT	ISC	FF	FFT	EFF	EFFT	BT	IRR
OCLI004001	.580	.582	1,240.	.702	.702	.113	.113	25.9	99.6
OCLI004002	.578	.581	1,230.	.677	.677	.108	.109	26.3	99.1
OCLI004003	.579	.581	1,220.	.697	.697	.109	.109	26.1	100.0
OCLI004004	.579	.582	1,250.	.683	.683	.109	.110	26.4	100.0
OCLI004005	.577	.580	1,240.	.683	.683	.109	.110	26.3	99.5
OCLI004006	.579	.583	1,240.	.690	.690	.110	.111	26.8	100.0
OCLI004007	.577	.581	1,240.	.682	.682	.108	.109	26.9	100.0
OCLI004008	.576	.580	1,260.	.670	.670	.109	.110	27.0	99.3
OCLI004009	.571	.573	1,170.	.683	.683	.102	.102	26.0	99.8
OCLI004010	.573	.576	1,190.	.679	.679	.104	.105	26.3	99.6
OCLI004011	.567	.570	1,130.	.675	.676	.096	.097	26.5	100.0
OCLI004012	.577	.580	1,200.	.697	.697	.107	.108	26.7	100.0
OCLI004013	.577	.581	1,240.	.664	.664	.105	.106	26.8	100.0
OCLI004014	.577	.581	1,220.	.697	.697	.109	.110	26.9	100.0
OCLI004015	.569	.572	1,180.	.671	.671	.100	.101	26.5	99.6
OCLI004016	.576	.580	1,170.	.713	.713	.107	.108	26.9	100.0
OCLI004017	.576	.580	1,300.	.676	.676	.113	.114	26.9	99.6
OCLI004018	.575	.579	1,250.	.694	.694	.111	.112	26.9	100.0
OCLI004019	.576	.580	1,240.	.698	.698	.111	.112	27.1	100.0
OCLI004020	.576	.580	1,230.	.692	.692	.110	.111	27.1	99.8
OCLI004021	.566	.570	1,160.	.686	.687	.100	.101	27.1	100.0
OCLI004022	.578	.582	1,210.	.728	.728	.113	.114	27.2	100.0
OCLI004023	.577	.582	1,230.	.699	.699	.110	.111	27.6	100.0
OCLI004024	.577	.582	1,240.	.707	.707	.113	.114	27.7	99.8
OCLI004025	.576	.581	1,220.	.703	.703	.109	.110	27.5	100.0
OCLI004026	.566	.571	1,160.	.686	.687	.100	.101	27.6	99.7
OCLI004027	.576	.581	1,230.	.701	.701	.110	.111	27.7	100.0
OCLI004028	.569	.575	1,160.	.720	.720	.106	.107	27.8	100.0
OCLI004029	.575	.581	1,250.	.670	.670	.107	.108	27.8	101.0
OCLI004030	.569	.574	1,170.	.716	.716	.106	.107	27.7	100.0
OCLI004031	.569	.574	1,130.	.684	.685	.098	.099	27.5	100.0
OCLI004032	.573	.578	1,200.	.726	.726	.110	.111	27.5	100.0
OCLI004033	.574	.580	1,200.	.730	.730	.112	.113	27.8	100.0
OCLI004034	.575	.580	1,160.	.748	.748	.111	.112	27.6	99.9
OCLI004035	.569	.575	1,150.	.716	.717	.104	.105	27.8	99.9
OCLI004036	.575	.580	1,220.	.693	.693	.108	.109	27.6	99.9
OCLI004037	.572	.578	1,190.	.696	.697	.105	.106	27.8	100.0
OCLI004038	.573	.579	1,240.	.692	.692	.109	.110	27.8	100.0
OCLI004039	.576	.582	1,220.	.703	.703	.109	.110	27.8	101.0
OCLI004040	.575	.581	1,230.	.709	.709	.111	.112	27.8	100.0
OCLI004041	.571	.577	1,170.	.707	.708	.105	.106	27.8	100.0
OCLI004042	.570	.576	1,180.	.711	.711	.106	.107	28.0	100.0
OCLI004043	.573	.579	1,210.	.716	.716	.110	.111	27.9	100.0
OCLI004044	.573	.579	1,230.	.685	.685	.107	.108	28.0	100.0
OCLI004045	.573	.580	1,200.	.691	.692	.104	.105	28.3	101.0
OCLI004046	.573	.580	1,200.	.705	.705	.108	.109	28.4	100.0
OCLI004047	.574	.581	1,220.	.704	.704	.109	.110	28.5	100.0
OCLI004048	.574	.581	1,210.	.707	.707	.109	.110	28.5	100.0
OCLI004049	.574	.581	1,250.	.686	.686	.108	.109	28.4	102.0
OCLI004050	.574	.581	1,240.	.680	.680	.107	.108	28.4	101.0

TABLE 9. (Continued)

CELL NUMBER	VOC	VOT	ISC	FF	FFT	EFF	EFFT	pT	IRR
OCLI004051	.575	.580	1,210.	.708	.708	.107	.108	27.5	102.0
OCLI004052	.574	.580	1,190.	.713	.713	.106	.107	27.8	102.0
OCLI004053	.570	.576	1,220.	.637	.638	.098	.099	28.0	101.0
OCLI004054	.571	.577	1,190.	.699	.700	.105	.106	28.1	101.0
OCLI004055	.573	.579	1,220.	.693	.693	.107	.108	28.1	100.0
OCLI004056	.575	.581	1,260.	.682	.682	.109	.110	28.1	101.0
OCLI004057	.572	.578	1,200.	.710	.710	.108	.109	28.0	101.0
OCLI004058	.574	.580	1,250.	.699	.699	.111	.112	28.0	100.0
OCLI004059	.568	.574	1,190.	.692	.693	.104	.105	28.0	100.0
OCLI004060	.574	.580	1,240.	.691	.691	.108	.109	28.2	101.0
OCLI004061	.572	.578	1,250.	.671	.671	.106	.107	28.0	100.0
OCLI004062	.574	.580	1,230.	.716	.716	.112	.113	28.1	99.9
OCLI004063	.574	.580	1,190.	.731	.731	.110	.111	28.2	101.0
OCLI004064	.573	.579	1,160.	.724	.724	.108	.109	27.9	101.0
OCLI004065	.571	.577	1,200.	.689	.690	.105	.106	28.1	100.0
OCLI004066	.574	.580	1,220.	.700	.700	.108	.109	28.2	101.0
OCLI004067	.574	.580	1,200.	.694	.695	.106	.107	28.2	101.0
OCLI004068	.574	.581	1,190.	.736	.736	.112	.113	28.4	99.9
OCLI004069	.574	.581	1,200.	.720	.720	.109	.110	28.3	101.0
OCLI004070	.570	.577	1,190.	.699	.700	.105	.106	28.6	100.0
OCLI004071	.572	.579	1,240.	.671	.672	.106	.107	28.4	99.9
OCLI004072	.574	.581	1,240.	.692	.692	.109	.110	28.6	100.0
OCLI004073	.568	.575	1,160.	.704	.705	.102	.103	28.4	101.0
OCLI004074	.567	.573	1,140.	.721	.722	.103	.104	27.9	101.0
OCLI004075	.572	.578	1,210.	.688	.689	.105	.106	28.2	100.0
OCLI004076	.573	.579	1,210.	.706	.706	.109	.110	28.2	99.9
OCLI004077	.573	.580	1,240.	.696	.696	.110	.111	28.3	99.9
OCLI004078	.565	.572	1,120.	.681	.682	.095	.096	28.4	100.0
OCLI004079	.568	.575	1,190.	.665	.666	.100	.101	28.4	100.0
OCLI004080	.573	.580	1,230.	.708	.708	.111	.112	28.6	100.0
OCLI004081	.573	.580	1,200.	.721	.721	.110	.111	28.7	100.0
OCLI004082	.571	.578	1,210.	.691	.692	.105	.106	28.7	101.0
OCLI004083	.572	.579	1,240.	.692	.692	.109	.110	28.6	99.9
OCLI004084	.570	.577	1,180.	.723	.724	.106	.107	28.6	102.0
OCLI004085	.573	.580	1,240.	.707	.707	.111	.112	28.7	101.0
OCLI004086	.572	.579	1,210.	.704	.704	.107	.108	28.6	101.0
OCLI004087	.571	.578	1,210.	.709	.709	.109	.110	28.5	100.0
OCLI004088	.567	.574	1,150.	.688	.689	.099	.100	28.5	100.0
OCLI004089	.570	.577	1,160.	.733	.733	.108	.109	28.6	99.9
OCLI004090	.569	.576	1,150.	.739	.740	.106	.107	28.6	101.0
OCLI004091	.571	.578	1,240.	.698	.698	.109	.110	28.7	101.0
OCLI004092	.569	.576	1,190.	.696	.697	.104	.105	28.7	100.0
OCLI004093	.570	.578	1,190.	.713	.713	.108	.110	28.8	100.0
OCLI004094	.568	.575	1,150.	.704	.705	.102	.103	28.7	100.0
OCLI004095	.567	.575	1,160.	.689	.690	.100	.102	28.8	101.0
OCLI004096	.567	.575	1,130.	.725	.726	.104	.106	28.8	100.0
OCLI004097	.574	.581	1,240.	.712	.712	.112	.113	28.7	100.0
OCLI004098	.568	.576	1,190.	.701	.702	.105	.107	28.9	100.0
OCLI004099	.566	.576	1,150.	.720	.721	.104	.106	28.8	100.0
OCLI004100	.573	.580	1,220.	.694	.695	.107	.108	28.7	101.0

SECTION IV

PLANS FOR THE NEXT QUARTER

During the next quarter, we plan the following:

(1) Completion of cell processing for sequences I, II, and III with solar-grade wafers*.

(2) Assessment of the cost/performance of these three sequences.

(3) Lamination of 1x4-ft and 4x4-ft double-glass panels containing these cells.

(4) Process refinement and an updated cost analysis for the double-glass lamination process.

(5) Verification testing of the radiant-heated mass reflow solder assembly.

(6) Assessment of the overall program and preparation of a final report.

*As was initially documented in Quarterly Report No. 5 and confirmed this quarter, no significant quantities of EFG ribbon or web silicon will be delivered by the vendors (Mobil-Tyco Solar Corp., Waltham, MA and Westinghouse Electric Corp., Pittsburgh, PA) in time for processing the number of cells origonally planned. If sheet material is received before the end of this program, evaluations will be made of its compatibility with those process steps where problems related to the use of sheet silicon are anticipated.

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2. R. V. D'Aiello, Automated Array Assembly, Phase II, Quarterly Report No. 4, prepared under Contract No. 954868 for Jet Propulsion Laboratory, DOE/JPL-954868-78/4, October 1978.